WHAT IS CLAIMED IS:

1. An Ethernet media access control (MAC) interface connectable between an Ethernet controller and a circuit under test, comprising:

a data link circuit connectable to the Ethernet controller and the circuit under test, the data link transmitting and receiving data;

a command and control link circuit;

a clock generator system, receiving commands from the command and control link circuit and sending a first clock signal to the Ethernet controller, and a second clock signal to the circuit under test;

at least one independent interface converter, receiving a clock signal from the clock generating system, said converter also receiving data from the data link circuit, converting a data stream, and transmitting said converted data to the data link circuit; and

a mode select circuit, receiving a mode select signal from the command and control link circuit and sending an enable signal to a converter,

wherein the clock generator system manipulates the clock signal to an enabled converter to synchronize data transfer from the circuit under test to the Ethernet controller.

2. The interface of Claim 1, wherein the at least one converter is selected from the group consisting of a first converter, a second converter and a third converter, the first converter converting a media independent interface (MII) data stream to a serial media independent interface (SMII) data stream and also converting an SMII data stream to an MII data stream, the second converter converting an MII data stream to a gigabit media independent interface (GMII) and also converting a GMII data stream to an MII stream, and the third converter converting an MII data stream to an MII data stream.

3. The interface of Claim 1, further comprising a first MII connector connected to the data link circuit, and a second connector connected to the

data link circuit, said second connector selected from the group consisting of an MII connector, a GMII connector, and an SMII connector.

4. The interface of Claim 1, wherein the command and control link circuit receives and transmits signals selected from the group consisting of a master clock signal, a system clock signal, a reset signal and a mode select signal.

5. The interface of Claim 2, wherein the at least one independent interface converter comprises a first converter converting an MII data stream to a SMII data stream and also converting an SMII data stream to an MII data stream, a frequency of the first clock signal is substantially one-tenth a frequency of a master clock signal, a frequency of the second clock signal is one-half a frequency of the master clock signal, and the frequency of the clock signal to the first converter is one-half the frequency of the master clock signal.

6. The interface of Claim 2, wherein the at least one independent interface converter comprises a second converter converting an MII data stream to a GMII data stream and also converting an GMII data stream to an MII data stream, a frequency of the first clock signal is substantially one-half a frequency of a master clock signal, a frequency of the second clock signal is one-fifth a frequency of the master clock signal, and the frequency of the clock signal to the second converter is one-fourth the frequency of the master clock signal.

7. The interface of Claim 2, wherein the at least one independent interface converter comprises a third converter converting an MII data stream to a MII data stream, a frequency of the first clock signal is one-half a frequency of a master clock signal, a frequency of the second clock signal is one-half a frequency of the master clock signal, and the frequency of the clock

signal to the third converter is one-half the frequency of the master clock signal.

8. The interface of Claim 5, further comprising an SMII crossover cable connecting said first converter with the data link circuit.

9. The interface of Claim 6, further comprising a GMII crossover cable connecting said second converter with the data link circuit.

10. The interface of Claim 7, further comprising an MII crossover cable connecting said third converter with the data link circuit.

11. A method of converting data from a circuit with an Ethernet controller, the method comprising:

connecting at least one independent interface converter to the circuit, to the Ethernet controller, and to a command and control center;

transmitting and receiving data among the circuit, the interface converter, and the Ethernet controller; and

synchronizing the transmitting and receiving by adjusting clock signals to the circuit, the interface converter, and the Ethernet controller,

wherein the data from the circuit is in a format selected from the group consisting of media independent interface (MII), serial media independent interface (SMII), and gigabit media independent interface (GMII).

12. The method of Claim 11, wherein the Ethernet controller receives and transmits data in an MII format.

13. The method of Claim 11, wherein the method further comprises synchronizing by using a fraction of a frequency of a master clock signal as a clock signal to the circuit under test.

14. The method of Claim 11, wherein the method further comprises synchronizing by stopping and starting said clock signals.

15. The method of Claim 11, wherein the method further comprises selecting a mode, wherein selecting the mode also selects a format for an independent interface.

16. A method of testing a circuit, the method comprising:
furnishing a circuit;
connecting the circuit to an independent interface converter;
synchronizing the circuit with the converter;
transmitting and receiving data from the circuit and the converter; and
controlling the circuit with an Ethernet LAN controller,
wherein the controller tests the circuit by synchronizing a speed of the Ethernet LAN controller with a speed of the circuit and wherein data from the device is in a format selected from the group consisting of a media independent interface (MII), a serial media independent interface (SMII), and a gigabit media independent interface (GMII).

17. The method of Claim 16, wherein the synchronizing occurs by furnishing a first clock signal to the Ethernet LAN controller, a second clock signal to the converter, and a third clock signal to the circuit.

18. The method of Claim 17, wherein the synchronizing occurs by stopping and starting a clock for at least one of said first, second and third clock signals.

19. The method of Claim 17, further comprising wherein the method further comprises selecting a mode, wherein selecting the mode also selects a format for an independent interface.

20. The method of Claim 16, wherein the Ethernet controller receives and transmits data in an MII format.

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